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CLAIMS 1-23 ARE CANCELED.

24. (currently amended) An integrated circuit comprising:

- a. a lateral NPN transistor having an emitter ~~electrode~~, a base ~~electrode~~, and a collector ~~electrode~~, the NPN transistor operable to conduct current between the emitter ~~electrode~~ and the collector ~~electrode~~ upon a positive first avalanche voltage applied between the emitter ~~electrode~~ and collector ~~electrode~~;
- b. an input element operable to receive a input voltage;
- c. a circuitry connected to the input element and to the NPN transistor;
- d. an NMOS transistor, having a source ~~electrode~~, a drain ~~electrode~~, and a gate ~~electrode~~, coupled to the lateral NPN transistor;
- e. the gate ~~electrode~~ capacitively coupled to input element and resistively coupled to a ground to maintain a voltage corresponding to the input voltage;

- f. the NMOS operable to conduct a drain current upon an electrostatic-discharge voltage less positive than the first avalanche voltage applied to the input element, the electrostatic-discharge voltage being more positive than the ordinary operating voltage of the circuitry coupled to the input element;
 - g. a lateral PNP transistor, having an emitter ~~electrode~~, a base ~~electrode~~, and a collector ~~electrode~~, connected to the input element and resistively coupled to the ground; and
 - h. the lateral PNP transistor operable to conduct a collector current upon an electrostatic-discharge voltage less positive than the first avalanche voltage applied to the input element, the electrostatic-discharge voltage being more positive than the ordinary operating voltage of the circuitry coupled to the input element, the collector current setting a base voltage at the base ~~electrode~~ of the lateral NPN transistor.
25. (new) The integrated circuit in claim 24, further comprising a p-doped element disposed near the base of the lateral NPN transistor, the p-doped element connecting the collector of the lateral PNP transistor and distancing the lateral NPN transistor from the lateral PNP transistor to maintain a SCR-free operation.
26. (new) The integrated circuit in claim 25, in which the NPN transistor includes a plurality emitter elements coupled in parallel, a plurality of base elements coupled in parallel, a plurality of collector elements coupled in parallel, and the p-doped element includes a plurality of p-doped sub-elements coupled in parallel.

27.(new) An integrated circuit comprising:

- a. a lateral NPN transistor having an emitter, a base, and a collector, the NPN transistor operable to conduct current between the emitter electrode and the collector electrode upon a positive first avalanche voltage applied between the emitter and collector;**
- b. an input element operable to receive a input voltage;**
- c. a circuitry connected to the input element and to the NPN transistor;**
- d. an NMOS transistor, having a source, a drain, and a gate, coupled to the lateral NPN transistor;**

- e. the gate capacitively coupled to input element and resistively coupled to a ground to maintain a voltage corresponding to the input voltage;
 - f. the NMOS operable to conduct a drain current upon an electrostatic-discharge voltage less positive than the first avalanche voltage applied to the input element, the electrostatic-discharge voltage being more positive than the ordinary operating voltage of the circuitry coupled to the input element;
 - g. a PMOS transistor, having an source, a gate, and a drain, connected to the input element and resistively coupled to the ground; and
 - h. the PMOS transistor operable to conduct a drain current upon an electrostatic-discharge voltage less positive than the first avalanche voltage applied to the input element, the electrostatic-discharge voltage being more positive than the ordinary operating voltage of the circuitry coupled to the input element, the drain current setting a base voltage at the base of the lateral NPN transistor.
- 28.(new) The integrated circuit in claim 27, further comprising a p-doped element disposed near the base of the lateral NPN transistor, the p-doped element connecting the collector of the lateral PNP transistor and distancing the lateral NPN transistor from the PMOS transistor to maintain a SCR-free operation.
- 29.(new) The integrated circuit in claim 28, in which the NPN transistor includes a plurality emitter elements coupled in parallel, a plurality of base elements coupled in parallel, a plurality of collector elements

coupled in parallel, and the p-doped element includes a plurality of p-doped sub-elements coupled in parallel.

30.(new) An integrated circuit comprising:

- a. a lateral NPN transistor having an emitter , a base , and a collector , the NPN transistor operable to conduct current between the emitter and the collector upon a positive first avalanche voltage applied between the emitter and collector ;
- b. an input element operable to receive a input voltage;
- c. a circuitry connected to the input element and to the NPN transistor;
- d. an NMOS transistor, having a source , a drain , and a gate , coupled to the lateral NPN transistor;
- e. the gate capacitively coupled to input element and resistively coupled to a ground to maintain a voltage corresponding to the input voltage;
- f. the NMOS operable to conduct a drain current upon an electrostatic-discharge voltage less positive than the first avalanche voltage applied to the input element, the electrostatic-discharge voltage being more positive than the ordinary operating voltage of the circuitry coupled to the input element;
- g. a vertical PNP transistor, having an emitter , a base , and a collector , connected to the input element and resistively coupled to the ground; and
- h. the vertical PNP transistor operable to conduct a collector current upon an electrostatic-discharge voltage less positive than the first avalanche voltage applied to the input element,

the electrostatic-discharge voltage being more positive than the ordinary operating voltage of the circuitry coupled to the input element, the collector current setting a base voltage at the base of the lateral NPN transistor.

31. (new) The integrated circuit in claim 30, further comprising a p-doped element disposed near the base of the lateral NPN transistor, the p-doped element connecting the collector of the vertical PNP transistor and distancing the lateral NPN transistor from the vertical PNP transistor to maintain a SCR-free operation.
32. (new) The integrated circuit in claim 31, in which the NPN transistor includes a plurality emitter elements coupled in parallel, a plurality of base elements coupled in parallel, a plurality of collector elements coupled in parallel, and the p-doped element includes a plurality of p-doped sub-elements coupled in parallel.